Abstract of the Disclosure:

A memory circuit, in particular a psuedostatic memory circuit, is selected by a memory selection signal. The memory circuit has memory areas and a control circuit in order to refresh a memory area of the memory circuit in accordance with a refresh request signal. The control circuit, in a first operating mode, carries out a refresh of the memory area at a refresh address after reception of the refresh request signal by generation of a refresh signal if the memory circuit is deselected or if, in the event of selection of the memory circuit by the memory selection signal, the access to the memory area is ended before the generation of a further refresh request signal. The control circuit, in a second operating mode, interrupts an access to the memory area for the writing and read-out of data and carries out a refresh of the memory area by generation of a refresh signal if the memory circuit is selected and a further refresh request signal is received before the ending of the access to the memory area.

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